REMARKS

Claims 1 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as invention. Claims 1, 3, 7, 9, 10, 11, 12, and 19 are rejected under 35 U.S.C. 102(b), as being anticipated by Imai. Claims 2 is rejected under 35 U.S.C 103(a) as being unpatentable over Imai in view of Fitch et al. (U.S. Pat. 5,213,989). Claims 4, 5, 13, and 14 are rejected under 35 U.S.C 103(a) as being unpatentable over Imai in view of Chuang et al. (U.S. PGPub 2003/0096486). Claims 6 and 15 are rejected under 35 U.S.C 103(a) as being unpatentable over Imai in view of Jambotkar. Claims 8 is rejected under 35 U.S.C 103(a) as being unpatentable over Imai in view of Oda et al. (U.S. Pat. 6,521,974).

1. Objection to the drawings:

The drawings are objected to under 37 CFR 1.83 (a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation "the dielectric layer is a shallow isolation trench (STI) oxide layer, and the predetermined region is a STI region" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Response:

The limitation "the dielectric layer is a shallow isolation trench (STI) oxide layer, and the predetermined region is a STI region" has been canceled from the claims. No new matter is entered. Allowance of the drawings is politely requested.

2. Rejection of claims 1 and 11 under 35 U.S.C. 112:

In regards to claim 1, the limitation "intrinsic base doped region" renders the claim indefinite. It is unclear what is meant by this limitation since an intrinsic region is a region with a negligible amount of impurities (undoped).

In regards to claims 1 and 11, the limitation "an emitter conductivity layer being filled with the self-aligned emitter region" renders the claims indefinite. For the purpose of this Office Action, it is considered the self-aligned emitter region is filled with an emitter conductivity layer.

Response:

As shown in Imai's disclosure (U.S. Pat. 5,506,427) recited by the Examiner, a p-type SiGe layer 36 with impurity concentration of 1×10^{18} to 1×10^{19} cm^{-3} is formed by a selective epitaxial growth technique and the p-type SiGe layer 36 serves as an p-type intrinsic base 36 (col.3, lines 62-65, & col.4, lines 1-2). Therefore, the limitation "intrinsic base doped region" of the claim 1 is an essential element of a bipolar junction transistor (BJT), and it does not render the claim 1 indefinite.

Additionally, in the amend d claims 1 and 11, the limitation "an emitter conductivity layer being filled with the self-aligned emitter region" has been replaced with "an emitter conductivity layer being filled into the self-aligned emitter region". No new matter is introduced. Allowance of the amended claims 1 and 11 is hereby requested.

3. Rejection of claims 1 and 5-8 under 35 U.S.C. 102(b):

In regards to claim 1, as best the examiner can ascertain the claimed invention, Figure 2 of Imai discloses a bipolar junction transistor (BJT) comprising: a substrate 14; a dielectric layer (20, 16) formed on a predetermined region of the substrate; an opening formed in the dielectric layer, and a portion of the substrate being exposed; a heavily doped polysilicon layer 32 formed on a sidewall of the opening to define a self-aligned base region (32, 30a, 36) in the opening; an intrinsic base doped region 36 formed within the substrate and in a bottom of the opening by implanting through the self-aligned base region; a spacer 34 formed on the heavily doped polysilicon layer to define a self-aligned emitter region in the opening; and an emitter conductivity layer (38, 40) being filled with the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the intrinsic base doped region (column 4, lines 12-15).

In regards to claim 3, Imai discloses the substrate 14 is silicon (column 3, lines 1-3).

In r gards to claim 7, Figur 2 of Imai discloses an extended conductivity layer 22 formed on the dielectric layer (20/16) electrically connected to the heavily doped polysilicon layer.

In regards to claim 9, Imai disclose the extended conductivity layer is composed of in-situ doped polysilicon (column 3, lines 5-15).

In regards to claim 10, Figure 2 of Imai discloses the dielectric layer 16 is a shallow isolation trench (STI) oxide layer, and the predetermined region is a STI region.

In regards to claim 10, Figure 2 of Imai discloses a hetero-junction bipolar junction transistor (HBT) comprising: a substrate 14; a dielectric layer (20, 16) formed on a predetermined region of the substrate; an opening formed in the dielectric layer, and a portion of the substrate being exposed; a SiGe epitaxial layer (30a, 36) (column 3, lines 39-65) formed on a sidewall and a bottom of the opening; a spacer 34 formed on the SiGe epitaxial layer to define a self-aligned emitter region in the opening; and an emitter conductivity layer (38, 40) being filled with the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the SiGe epitaxial layer (column 4, lines 12-15).

In regards to claim 12, Imai discloses the substrate 14 is a silicon substrate (column 3, lines 1-3).

In regards to claim 10, Figure 2 of Imai discloses the dielectric layer 16 is a shallow isolation trench (STI) oxid layer, and th pr det rmined r gion is a STI region.

Response:

The amended claim 1 is amended according to Figs.6-9. No new matter is introduced. The amended claim 1 of the present application is repeated below:

"1. A bipolar junction transistor (BJT) comprising:
a substrate;
a dielectric layer formed on a predetermined region of the substrate;
an oxide layer and a silicon nitride layer stacked on the dielectric layer;
an opening formed in the dielectric layer, the oxide layer, and the silicon nitride layer, a portion of the substrate being exposed;
a heavily doped polysilicon layer formed on a sidewall of the opening and on the substrate to define a self-aligned base region in the opening;
an intrinsic base doped region formed within the substrate and in a bottom of the opening by implanting through the self-aligned base region;
a spacer formed on the heavily doped polysilicon layer to define a self-aligned emitter region in the opening; and
an emitter conductivity layer being filled ~~with~~ into the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the intrinsic base doped

region."

As described in the amended claim 1 and Figs.8-9, an opening 98 is formed in a dielectric layer84, an oxide layer 92, and a silicon nitride layer 94, and a heavily doped polysilicon layer 104 is formed on a sidewall of the opening 98 and on the substrate 74. That is, the heavily doped polysilicon layer 104 is formed <u>on the sidewalls of the dielectric layer 84, the oxide layer 92, and the silicon nitride layer 94, and on the surface of the substrate 74</u>.

However, Imai discloses that the P^+-type polysilicon film 32 is formed on <u>the sidewall of the oxide film 20 and on the surface of the P^+-type external base 30a</u> (Fig.2, col.3, lines 8-14, & col. 3, lines 44-50). Therefore, the structure taught in the amended claim 1 of the present application should be definitely different from that disclosed in Imai's disclosure. Reconsideration of the amended claim 1 is hereby requested.

Additionally, the amended claim 11 is amended through emerging the claim 16 into the claim 11. No new matter is introduced. The amended claim 11 of the present application is repeated below:

"11. A hetero-junction bipolar junction transistor (HBT) comprising:

a substrate;

a dielectric layer formed on a predetermined region of the substrate;

an opening formed in the dielectric layer, and a portion of the substrate being exposed;

a Si e epitaxial layer formed on a sidewall and a bottom of the opening, and extending outside the opening and above the dielectric layer;

a spacer formed on the SiGe epitaxial layer to define a self-aligned emitter region in the opening; and

an emitter conductivity layer being filled into the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the SiGe epitaxial layer."

As described in the amended claim 11 and Figs.12-14 of the present application, the SiGe epitaxial layer 103 is formed on a sidewall and a bottom of the opening 98, and the SiGe epitaxial layer 103 extends outside the opening 98 and above the dielectric layer including a silicon dioxide layer 92 and a silicon nitride layer 94.

Nevertheless, as shown in Figs.1-2 of Imai's disclosure, the P-type SiGe layer 36 is positioned on the bottom of the opening 25 and the P-type SiGe layer 36 does not extend outside the opening 25. Accordingly, the structure taught in the amended claim 11 of the present application should be definitely different from that disclosed in Imai's disclosure. Reconsideration of the amended claim 11 is hereby requested.

As claims 3, 7, and 9 are dependent upon the amended claim 1, they should be allowed if the amended claim

1 is allowed. Likewise, since the claim 12 is dep nd nt upon the mended claim 11, it should be allowed if the amended claim 11 is allowed. Reconsideration of the claims 3, 7, 9, and 12 is hereby requested.

5. Rejection of claim 2 under 35 U.S.C. 103(a):

In regards to claim 2, the difference between Imai and the claimed invention is the heavily doped polysilicon layer is doped with a boron dopant. Fitch discloses boron is conventionally used as a p-type dopant (column 7, lines 5-8). The heavily doped region 32 of Imai is p-type. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Imai by using boron as the dopant in the heavily doped polysilicon region for the purpose of obtaining a p-type region. A further difference between Imai and the claimed invention is the dosage ranging from 1E19 to 1E21. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of by, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. The ordinary artisan would have been motivated to modify in the manner described above for the purpose of decreasing resistance of the base electrode.

Response:

As claim 2 is dependent upon the amended claim 1, it should be allowed if the amended claim 1 is allowed.

Reconsideration of the claim 2 is hereby requested.

6. Rejecti n of claims 4, 5, 13 and 14 under 35 U.S.C. 103(a):

In regards to claims 4 and 13, the difference between Imai and the claimed invention is the substrate is a non-selective epitaxial substrate. Figure 1A of Chuang discloses a non-selective epitaxial substrate 102. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Imai by using a selective deposition method layer for the epitaxial substrate. The ordinary artisan would have been motivated to modify in the manner described above for the purpose of depositing epitaxial layer.

In regards to claims 5 and 14, the difference between Imai and the claimed invention is a silicide layer formed on the emitter conductivity layer. Figure 2H of Chuang discloses a silicide layer 222 formed on an emitter conductivity layer 212a. In view of such teaching, it would have been the ordinary artisan at the same time was made to modify the invention of Imai by including a salicide layer on the emitter conductivity layer for the purpose of decreasing the contact resistance.

Response:

As claims 4 and 5 are dependent upon the amended claim 1, they should be allowed if the amended claim 1 is allowed. Likewise, since claims 13 and 14 are dependent upon the amended claim 11, they should be allowed if the amended claim 11 is allowed.

Reconsid ration of th claims 4-5 and 13-14 is h reby requested.

7. Rejection of claims 6 and 15 under 35 U.S.C. 103(a):

In regards to claims 6 and 15, the difference between Imai and the claimed invention is a selective implant collector (SIC) region formed in the substrate beneath the intrinsic base doped region. Figure 1B of Jambotkar discloses a SIC region 31 below an intrinsic base region 33. In view of such teaching, it would have been the ordinary artisan at the same time was made to modify the invention of Imai in the manner described above for the purpose of minimizing the series collector resistance.

Response:

As claims 6 and 15 are dependent upon the amended claim 1 and the amended claim 11 respectively, they should be allowed if the amended claim 1 and the amended claim 11 are allowed. Reconsideration of the claims 6 and 15 is hereby requested.

8. Rejection of claim 8 under 35 U.S.C. 103(a):

In regards to claim 8, the difference between Imai and the invention is an oxide layer and a silicon nitride layer formed between the extended conductivity layer and the dielectric layer. Figure 1 of Oda discloses an oxide layer 7 and a silicon nitride layer 8 formed between an extended conductivity layer 9 and a dielectric layer 4. In view of such teaching, it would have been the ordinary artisan at the same time was made to modify the invention of Imai by including the

oxide and nitrid layers f Oda for the purpos of providing additional isolation from the substrate.

Response:

The claim 8 is canceled because it has been emerged into the claim 1.

9. Allowance of claim 16:

Claim 16 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response:

The claim 16 is canceled because it has been emerged into the claim 11. Reconsideration of the amended claim 11 is hereby requested.

Sincerely yours,

Winston Hsu Date: 9/24/2003

Winston Hsu, Patent Agent No.41,526
P.O. BOX 506
Merrifield, VA 22116
U.S.A.
e-mail: winstonhsu@naipo.com.tw